

PCS3P2537A

Product Preview

Peak EMI Reduction IC

Product Description

PCS3P2537A is a 1x spread spectrum frequency modulator designed to reduce electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The device allows significant system cost savings by reducing the number of circuit board layers, ferrite beads and shielding and other passive components that are traditionally required to pass EMI regulations.

PCS3P2537A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This result in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’.

PCS3P2537A has a frequency range of 18 MHz – 36 MHz, and accepts input clock either from a Crystal or from an external reference and locks on to it delivering a 1x spread spectrum clock output. It has an SSON control for enabling and disabling Spread Spectrum function.

PCS3P2537A operates with a supply voltage of 3.3 V, and is available in 8 L–WDFN package.

Application

PCS3P2537A is targeted towards PC peripheral devices and embedded systems.

General Features

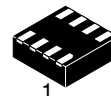
- 1x Peak EMI Reduction IC
- Input Frequency: 18 MHz – 36 MHz
- Output Frequency: 18 MHz – 36 MHz
- Frequency Deviation @ 27 MHz: -0.25%
- Modulation Rate @ 27 MHz: 30.1 KHz
- Supply Voltage: 3.3 V ± 0.3 V
- Operating Current less than 8 mA @ 27 MHz
- Spread Spectrum Enable Control
- CMOS Design
- 8L–WDFN (8L–TDFN) Package
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.



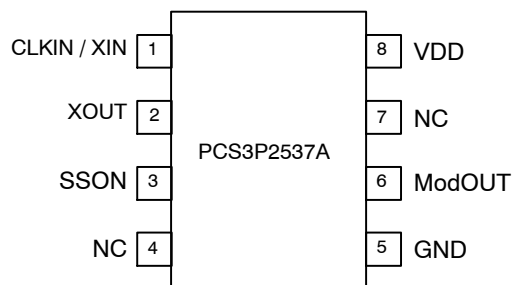
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WDFN8 2x2, 0.5P
CASE 511AQ

PIN CONFIGURATION



(8L–WDFN Package)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

PCS3P2537A

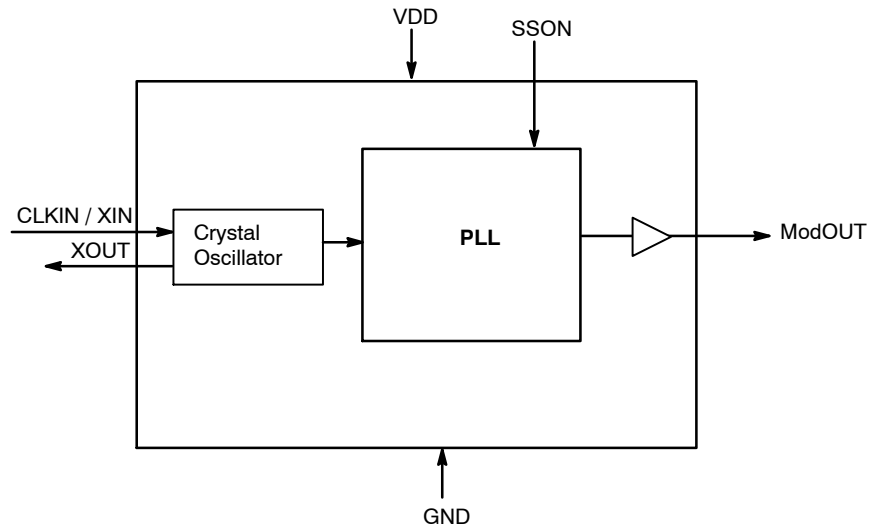


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	CLKIN / XIN	Input	External reference Clock input or Crystal connection. This pin has dual functions. It can be connected either to an external crystal or an external reference clock.
2	XOUT	Output	Crystal connection. If using an external reference, this pin must be left unconnected.
3	SSON	Input	When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum.
4	NC		No Connect.
5	GND	Power	Ground Connection.
6	ModOUT	Output	Spread Spectrum Clock Output.
7	NC		No Connect.
8	VDD	Power	Power supply for the entire chip.

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V _{IN}	Voltage with any pin with respect to Ground	-0.5 to +4.6	V
T _{STG}	Storage temperature	-65 to +125	°C
T _s	Max. Soldering Temperature (10 sec)	260	°C
T _J	Junction Temperature	150	°C
T _{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. OPERATING CONDITIONS

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
T _A	Operating Temperature (Ambient Temperature)	0	70	°C
C _L	Load Capacitance		15	pF
C _{IN}	Input Capacitance		7	pF

PCS3P2537A

Table 4. DC ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY

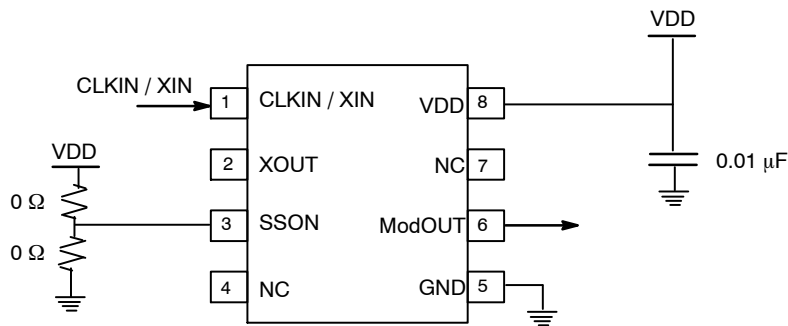
Symbol	Parameter	Min	Typ	Max	Units
V _{IL}	Input low voltage	VSS – 0.3		0.8	V
V _{IH}	Input high voltage	2.0		VDD + 0.3	V
I _{IL}	Input low current			–35	μA
I _{IH}	Input high current			35	μA
V _{OL}	Output low voltage (VDD = 3.3 V, I _{OL} = 8 mA)			0.4	V
V _{OH}	Output high voltage (VDD = 3.3 V, I _{OH} = 8 mA)	2.5			V
I _{DD}	Static supply current (Note 1)			2.5	mA
I _{CC}	Dynamic supply current (3.3 V, 27 MHz and no load)		5	8	mA
VDD	Operating Voltage	3	3.3	3.6	Ω
t _{ON}	Power-up time (first locked cycle after power-up)			5	mS
Z _{OUT}	Output impedance		36		Ω

1. CLKIN is pulled to GND.

Table 5. AC ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY

Symbol	Parameter	Min	Typ	Max	Units
CLKIN	Input frequency	18	27	36	MHz
ModOUT	Output frequency	18	27	36	MHz
f _d	Frequency Deviation @ 27 MHz	–0.2	–0.25	–0.3	%
MR	Modulation Rate @ 27 MHz	30		33	KHz
t _{LH} (Note 2)	Output rise time (measured from 20% to 80%)			2	nS
t _{HL} (Note 2)	Output fall time (measured at 80% to 20%)			1.5	nS
t _{JC}	Cycle-to-Cycle Jitter at 27 MHz		±200	±300	pS
t _D	Output duty cycle	45	50	55	%

2. t_{LH} and t_{HL} are measured into a capacitive load of 15 pF.



Note: Refer to Pin Description table for Functionality Details.

Figure 2. Typical Application Schematic

PCS3P2537A

PCB Layout Recommendation

For optimum device performance, the following guidelines are recommended.

- Dedicated VDD and GND planes.
- The device must be isolated from system power supply noise. A 0.01 μ F decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The

PCB trace to VDD pin and the ground via should be kept as short as possible. All the VDD pins should have decoupling capacitors.

- In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

A typical layout is shown in the Figure 3.

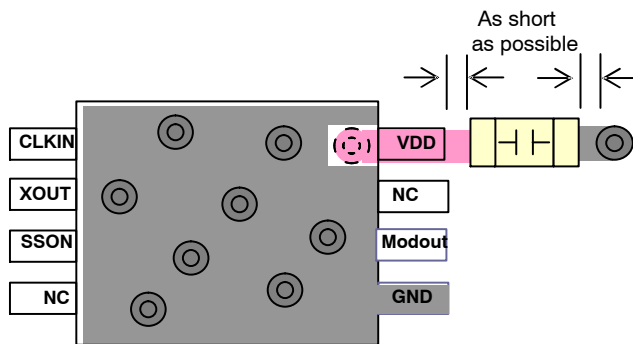
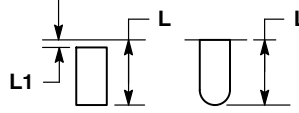
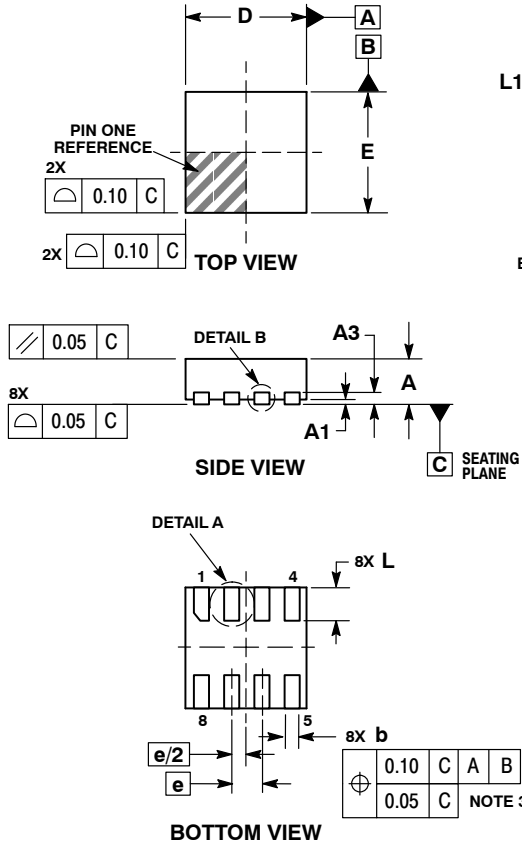


Figure 3. Typical Layout

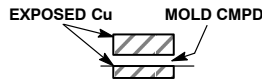
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PACKAGE DIMENSIONS

WDFN8 2x2, 0.5P
CASE 511AQ
ISSUE A



DETAIL A
OPTIONAL
CONSTRUCTIONS



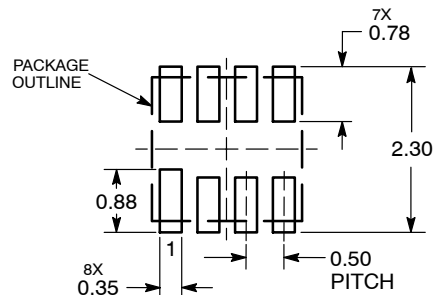
DETAIL B
OPTIONAL
CONSTRUCTION

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.50	0.60
L1	---	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PCS3P2537A

Table 6. ORDERING INFORMATION

Part Number	Top Marking	Package Type	Temperature
PCS3P2537AG-08CR	AM	8L-WDFN (8L-TDFN) – TAPE & REEL, Green	0°C to +70°C

NOTE: A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free

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